

VLSI AND GRAPHICS AT THE PIXEL LEVEL*

Henry Fuchs

Department of Computer Science
University of North Carolina
Chapel Hill, North Carolina 27514

Abstract

The computational bottlenecks in many interactive raster graphics systems are the pixel-level calculations and not the display list traversals, geometric transformations or clipping computations. We examine several VLSI-based designs that focus on these pixel-level calculations, noting the influence of the price-performance target on system design and component selection. We describe in detail the latest results from *Pixel-planes*, our experimental system optimized for algorithms in which many of the pixel-level calculations can be formulated as linear expressions ($Ax + By + C$) of the pixel's x, y address. We outline variations on the current implementation for greater generality or faster speed or lower cost. We show the effects of these changes on the algorithms that are to be run on the alternative implementations.

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