# Real-Time Image Edge Extraction with Integrated CMOS Sensors

Denis Dubois
Denis Poussart

Laboratoire de Vision et Systèmes Numériques
Département de Génie Electrique
Université Laval,
Québec, Canada, G1K 7P4

## Abstract

This paper describes two models of a real-time edge extracting system implemented in VLSI CMOS technology. Each unit is complete and include processing circuitry as well as photosensitive devices which perform light acquisition directly from a scene. The first model (LVRET) uses an algorithm which is based on principles of lateral inhibition and the second one (LVHEX) takes advantage of the behavior of a large resistive network as a smoothing operator. The circuits are built upon an hexagonal tessellation and their output is derived from a scanning operation performed on a 28 x 36 planar array in the LVRET chip and 27 x 35 in the LVHEX one. The paper outlines some basic concepts which arise from biological and neuronal architecture and describes how the relevant concepts mesh with the intrinsic properties of VLSI.

## Resumé

Cet article présente deux modèles de systèmes d'extraction d'arêtes en temps réel realisés sur circuits intégrés à très grande échelle. Les unités ne nécessitent pas de caméra puisque les éléments de calcul ainsi que les photosenseurs qui recoivent l'information lumineuse directement de la scène sont inclus sur le même substrat de silicium. Le premier modèle (LVRET) utilise un algorithme décisionnel derivé du principe d'inhibition latérale tandis que le second (LVHEX) exploite l'effet d'adoucissement de signal d'un grand réseau resistif. Une tessellation hexagonale est utilisée pour couvrir tout le plan image et la sortie est le résultat du balayage d'une matrice de 28 x 36 pixels pour LVRET et de 27 x 35 pour LVHEX. L'article expose les principes architecturaux inspirés des systèmes biologiques et illustre comment ceux-ci s'intègrent naturellement et efficament à la technologie microélectronique.

**Keywords:** Integrated sensing, analog VLSI implementation, edge detection, parallel computing, photosensitive silicon devices.

## Introduction

With the recent developments in the area of semiconductors, it has become increasingly apparent that very complex, special purpose systems can be implemented on a single chip and that different types of devices can be integrated on the same silicon wafer. In order to obtain the very high levels of density and high speed necessary for real-time implementation of computer vision algorithms, one must take full advantage of the intrinsic properties of conventional silicon devices. This translates into two observations: *i)* typically, analog circuitry which directly implements computations to be performed have significant advantages of processing speed over digital approaches and *ii)* global communications are very costly in terms of utilization of the silicon real estate, and therefore architectures with dense local connectivity must be priviledged. Biological systems follow similar principles, and vision in particular provides a very pertinent model of organization [12]. In the same spirit, it is logical to attempt an integration of the transducting and of the processing components in order to achieve high performance, "intelligent" sensing. The devices described in this paper combine photosensitive devices and analog elements on the same silicon chip [16], thus allowing direct data connections and providing a computation which proceeds in a massively parallel manner.

Neural networks models are good examples of the kinds of architectures which are directly inspired from studies of biological systems. These networks are complex, highly organized and fairly regular structures, and are composed of a large number of simple processors connected to one another, as in nervous tissue [9, 8, 1, 4]. The results presented here are very much influenced by neural network principles.

## Parallel Architecture

Typically, conventional, sequential computing is not capable of providing the level of performance required for real-time image processing. Although the speed of single digital devices is impressive, and far superior to that of biological elements, only a small fraction of the available ressources is utilized at any particular time and intensive tasks such as early-processing and recognition are overwhelming.

Vision processing is a field where a strategy of parallel architecture is most indicated. Indeed, *i)* the very nature of light is such that the incoming optical information impinges upon the sensor in a parallel manner and *ii)* the early processing operations to be performed involved a high degree of local support and connectivity. Therefore a sensing architecture which integrates light transduction within an array of local processors which have efficient communication with their surrounding neighbors has the required attributes and the potential of high performance. This is a path which Nature has largely developped.